ABSTRACT

In one embodiment, a trace buffer circuit for use with a pipelined digital signal processor (DSP) may include a series of interconnected registers that operate as a first-in first-out (FIFO) register on a write operation and a last-in first-out (LIFO) register on a read operation. On the write operation, a branch target/source address pair may be written to a first pair of trace buffer registers and, the contents of each register may be shifted two registers downstream. On the read operation, one instruction address may be read from a top register, and the contents of each register may be shifted one register upstream. The trace buffer may also include structure to enable compression of hardware and software loops in the program flow. A valid bit may be assigned to each instruction address in the trace buffer and a valid bit buffer with a structure parallel to that of the trace buffer may be provided to track the valid bits.